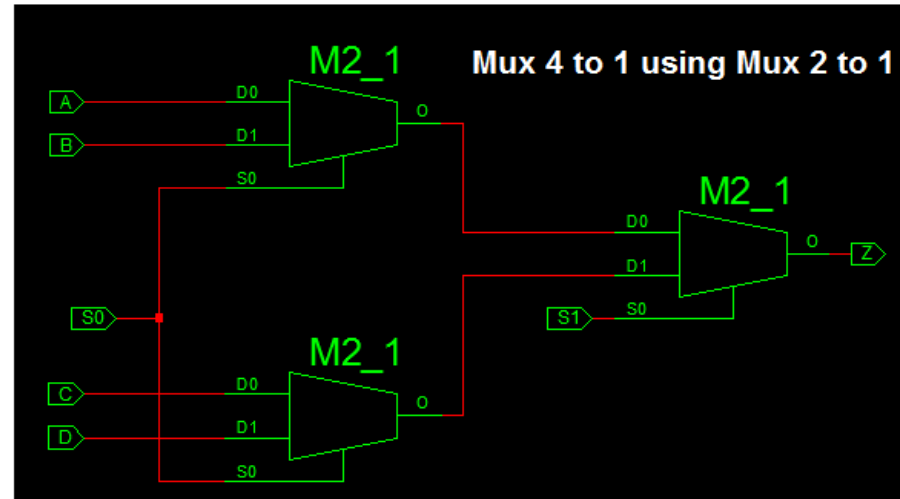


## 4 to 1 Mux Implementation using 2 to 1 Mux



### VHDL Code for 2 to 1 Mux

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity mux2_1 is
5  port(A,B : in STD_LOGIC;
6  S: in STD_LOGIC;
7  Z: out STD_LOGIC);
8  end mux2_1;
9
10 architecture Behavioral of mux2_1 is
11
12 begin
13
14 process (A,B,S) is
15 begin
16 if (S = '0') then
17 Z <= A;
18 else
19 Z <= B;
20 end if;
21 end process;
22
23 end Behavioral;

```

### VHDL 4 to 1 Mux using 2 to 1 Mux

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity mux4_1 is
5  port(
6
7  A,B,C,D : in STD_LOGIC;
8  S0,S1: in STD_LOGIC;
9  Z: out STD_LOGIC
10 );
11 end mux4_1;
12
13 architecture Behavioral of mux4_1 is
14 component mux2_1
15 port( A,B : in STD_LOGIC;
16 S: in STD_LOGIC;
17 Z: out STD_LOGIC);
18 end component;
19 signal temp1, temp2: std_logic;
20
21 begin
22 m1: mux2_1 port map(A,B,S0,temp1);
23 m2: mux2_1 port map(C,D,S0,temp2);
24 m3: mux2_1 port map(temp1,temp2,S1,Z);
25
26 end Behavioral;

```